REMARKS

I. Claim Rejection – 35 USC § 102

Claims 1 and 23-24 were rejected under 35 USC § 102 as being anticipated by Ovens. The method claims 23-24 have be canceled without prejudice and replace with new apparatus claims 28-32 directed to the converting circuit.

A. Description of Ovens and problem addressed

The prior art FIG. 1 of Owens describes an I/O section 102 having a clock source (not shown) providing a clock signal 100 to a clock level shifter 108. In the core section 104, clock signals CLKT and CLKF are used by a clock latch (flip-flop) 118 to latch data 120 and provide a data output 122 to a data level shifter 126. The described problem with this prior art circuit is that the time from the clock input of the clock 100 to the output node 128 is too long. In FIG. 2 of Ovens (now part of the Ovens invention), "the latch is moved from the core section to the I/O section, thereby removing the delay caused by level shifting the clock down to the core voltage for the latch. Generally, this has the effect of making the clock-to-Q time faster than the circuit of FIG. 1. Hence, in FIG. 2 of Ovens, a data signal 204 from the core section is level shifted by the data level shifter 206 to generate level shifted data 226, which is received by the latch 224 (Examiner refers to this as the latch in Box B) in the I/O section, where the clock source is located.

B. Applicant's Claimed invention addresses a different problem than Ovens

Applicant's invention, as claimed in independent claims, addresses a wholly different problem with different structure than either FIG. 1 or FIG. 2 of Ovens. Unlike the clock-to-Q time problem addressed in Ovens, Applicant's invention addresses the fact that voltage level shifters introduce extra timing skew between the rising and falling edges (signal transitions) of the data signals and clock signals, as shown by the cross hash lines in the "level shifted data" of FIG. 4 of Applicant's drawings. In other words, the data shifted signal has a time period during which the rising and falling data edges are mismatched. The triggering edge of the delayed clock signal for triggering the downstream latch is delayed by the delay element (now recited in all independent

claims) until after an arrival of the rising and falling data edges (signal transistions) at the of the downstream latch.

Paragraphs 18-20 (paragraph 21 is a summary) of Applicant's specification describes how the introduction of the downstream latch (downstream slave latch in independent claim 28) allows for the timing of the signal transistions of the output data signal of the downstream latch to be tied only to one clock edge instead of two edges, with the "triggering clock edge" for the downstream latch now being recited in all the independent claims. In the embodiments of FIGS. 1 and 2 of Ovens, the level shifted data signal from the voltage level shifter 126 and voltage level shifter 206, respectively, would have the same mismatching, but there is no teaching in Ovens that such mismatching would be reduced by a downstream latch triggered by one clock edge, the triggering clock edge.

C. Examiner's characterization of the latch (flip-flop) in Box B of Ovens

As stated in Ovens, "the term **latch** is defined to include a flip-flop" (see column 3, beginning line 31). Hence, the latch 118 in FIG. 1 and the latch 224 in Box B in FIG. 2 of Ovens are flip-flops. Moreover, the latches 118 and 224 are master-slave flip-flops having a master latch and a slave latch (see column 4, lines 55-56).

In the Examiner's rejection of all of Applicant's independent claims, the Examiner assumes that the "downstream latch" of Applicant's invention is the same as the flip-flop in Box B of FIG. 2 of Ovens. To the contrary, Applicant's downstream latch is not a flip-flop, but instead is a simple latch having an open state (transparent state) and a close state (non-transparent, hold or latch state).

To clear up any misunderstanding, all the independent claims have been amended to recite that the downstream latch (or downstream slave latch, depending upon the claim), has "an open state and a close state". Moreover, all the independent claims have been amended to recite that the downstream latch is triggered by a single "triggering clock edge" of the delayed clock signal. Unlike a master-slave flip flop, in the downstream latch of Applicant's invention, only one of the rising or falling edges of the

clock signal is used to trigger an open state, which is now recited in all the independent claims as the "triggering clock edge".

D. Distinctions of Independent claims 1, 10, 16, 21 and 28 over Ovens

Although Ovens teaches a flip-flop with a voltage level shifter being upstream or downstream of the flip-flop, Oven's does not teach:

(1) a flip-flop and a downstream latch having an open state and a close state, with the voltage level shifter interposed between the flip-flop and the downstream latch; and

(2) a delay element to delay the clock signal, with a triggering clock edge of the delayed clock signal being used to trigger the downstream latch.

In independent claim 28 the term "downstream slave latch" is used instead of "downstream latch"; however, this term is also used in original dependent claims 8, 14, and 21.

II. Claim Rejection – 35 USC § 103

The Examiner rejected claims 10-22 under 35 USC § 103(a) as being unpatentable over Ovens in view of Cairns. Later in the Examiner's response, the Examiner also rejects claims 2-9 and 25-27 as being unpatentable over Ovens and in further view of Cairns. Method claims 25-27 have been cancelled. The Examiner also provided a reference to Yepp, but this reference was not mentioned in the Examiner's rejection, nor does it appear relevant to Applicant's invention in that it only discloses master slave latch combinations. Hence, the Applicant will address the combination of Ovens and Cairns for all the claims mentioned above, with claims having the same or similar limitations being addressed together.

First, all the dependent claims are patentably distinct because they dependent from independent claims 1, 10, 16, and 28 and for the same reasons described in Section I.D. above, since neither Ovens or Cairns or the combination of the two references teach:

(1) a flip-flop and a downstream latch having an open state and a close state, with the voltage level shifter interposed between the flip-flop and the downstream latch; and

(2) a delay element to delay the clock signal, with a triggering clock edge of the delayed clock signal being used to trigger the downstream latch.

With respect to independent claims 10 and 16 and original dependent claim 2, the Examiner combines Cairns with Ovens, because Ovens does not teach the second level shifter, coupled to the clock source, for shifting the voltage level of the clock signal. Although Cairns may show a voltage level shifter for a clock signal, it does not teach a voltage level shifter for providing a clock signal to a single downstream latch having an open state and a close state. As pointed out by the Examiner, in Cairns the shifted clock signal is provided to a "latch circuit 44". As described in column 9, this is a "D-type latch". This D-type latch is a type of flip-flop having cross coupled gates.

With respect to original dependent claims 4, 11 and 18, Ovens does not teach does not teach a downstream latch with an open (transparent) state and a close (hold) state, but teaches an upstream or downstream flip-flop, as discussed above. This claim recitation is now incorporated into all of the independent claims.

With respect to original dependent claim 5, 12, and 19, Ovens does not disclose a delay element for delay the clock signal. Original dependent claims 5, 12, and 19 have been cancelled and incorporated into independent claims 1, 10, and 16 respectively. The Examiner refers to column 3, lines 43-50 of Ovens. Applicant cannot find any reference to delays in this paragraph; however, the next paragraph refers to the common practice of using buffers to equalize clock delays. Applicant's delay is wholly different, in that a delay is introduced between the flip-flop (more specifically, the upstream slave latch) and the downstream latch (downstream slave latch). This relative delay allows the downstream latch to transition to its open state after the upstream slave latch transitions to its open state so as to cut out the mismatching in the level shifted data signal.

With respect to original dependent claims 6, 13, and 20 (and new dependent claim 29), these claims more specifically describe the delay introduced by the delay element to be operable to delay an arrival of the triggering clock edge to the downstream

latch until after an arrival of the rising and falling data edges of the level shifted signal from the first level shifter. As explained in the previous paragraph, Ovens does not teach delaying the triggering clock edge until the arrival of the rising and falling data edges at the downstream latch. More specifically, the Examiner refers to column 5, lines 21-33 of Ovens. But this section merely refers to FIG. 3 and the merging of the master latch and the level shifter and how the master-slave flip-flop functions, without any reference to a downstream latch.

With respect to original dependent claims 8, 9, 14, 15, 21, and 22, these claims further defines the flip-flop as having a master latch and an upstream slave latch and that the downstream latch is a downstream slave latch. However, this terminology is helpful in understanding the invention; hence, the Applicant's have replaced the method claims 23-27 with new apparatus claims 28-32 using this master-slave language of the dependent claims.

With respect to original dependent claim 7, this is another way to express the delay introduced by the delay element; however, it presupposes the existence of the delay caused by the second level shifter. This language is also in new claim 32.

III. Conclusion

Claims 1-4, 6-11, 13-18, and 20-22 and new claims 28-32 are pending. Claims 5, 12, 19, 23-27 have been canceled. In view of the foregoing amendments and arguments, Applicant submits that the pending claims are in condition of allowance. Early issuance of Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,

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